CLAIMS

What is claimed is:

1. An apparatus comprising:

first and second bus interface circuits to interface to first and second buses, respectively, the first bus being accessible to a first processor;

a processor interface circuit to interface to a second processor; and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors.

2. The apparatus of claim 1 wherein the second processor is coupled to the first and second buses.

3. The apparatus of claim 2 wherein the processor interface circuit comprises:

a command decoder to decode an access command from the second processor requesting access to one of the first and second buses.

4. The apparatus of claim 1 wherein the arbitration logic circuit disables the first bus interface circuit when the second processor requests access to the second bus.

5. The apparatus of claim 1 wherein the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted.

6. The apparatus of claim 1 wherein the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

7. The apparatus of claim 1 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

8. The apparatus of claim 1 wherein the second processor is a direct memory access (DMA) controller.

9. The apparatus of claim 1 wherein the first and second buses are of same type.

10. The apparatus of claim 1 wherein the first and second buses are of different types.

11. A method comprising

interfacing to first and second buses by first and second interface circuits, respectively, the first bus being accessible to a first processor;

interfacing to a second processor; and

arbitrating access requests from the first and second processors.

12. The method of claim 11 wherein the second processor is coupled to the first and second buses.

13. The method of claim 12 wherein interfacing to the second processor comprises:

decoding an access command from the second processor requesting access to one of the first and second buses.

14. The method of claim 11 wherein arbitrating access requests comprises disabling the first bus interface circuit when access request to the second bus from the second processor is granted.

15. The method of claim 11 wherein arbitrating access requests comprises enabling the first and second bus interface circuits when access request to the second bus from the first processor is granted.

16. The method of claim 11 wherein arbitrating access requests comprises resolving the access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

17. The method of claim 11 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

18. The method of claim 11 wherein the second processor is a direct memory access (DMA) controller.

19. The method of claim 11 wherein the first and second buses are of same type.

20. The method of claim 11 wherein the first and second buses are of different types.

21. A system comprising:

first and second buses;

first and second processors, the first processor being coupled to the first bus;

a bus controller coupled to the first and second buses to control bus access from the first and second processors, the bus controller comprising:

first and second bus interface circuits to interface to the first and second buses, respectively,

a processor interface circuit to interface to the second processor, and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors.

22. The system of claim 21 wherein the second processor is coupled to the first and second buses.

23. The system of claim 22 wherein the processor interface circuit comprises:

a command decoder to decode an access command from the second processor requesting access to one of the first and second buses.

24. The system of claim 21 wherein the arbitration logic circuit disables the first bus interface circuit when the second processor requests access to the second bus.

25. The system of claim 21 wherein the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted.

26. The system of claim 21 wherein the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

27. The system of claim 21 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

28. The system of claim 21 wherein the second processor is a direct memory access (DMA) controller.

29. The system of claim 21 wherein the first and second buses are of same type.

30. The system of claim 21 wherein the first and second buses are of different types.